REMARKS

By this amendment, claims 1, 12, 13, and 14 have been amended. Claims 1-14 remain in the application. This application has been carefully considered in connection with the Examiner's Action. Reconsideration, and allowance of the application, as amended, is respectfully requested.

Rejection under 35 U.S.C. § 102

Claim 1

Claim 1 recites a data processing circuit for processing an input data pattern and for outputting an output data pattern, said data processing circuitry comprising:

a) estimation means for estimating a processing delay in response to said input data pattern, wherein the estimated processing delay corresponds to a delay that is caused as a function of a processing activity induced in said data processing circuit by said input data pattern; and

b) control means for controlling said processing of the input data pattern by said data processing circuit according to the processing activity of said data processing circuit in response to said estimated processing delay.

Support for the amendments to claim 1 (similarly, for claim 12), can be found in the specification on at least page 1, lines 28-29; and page 2, lines 1-44.

Claims 1, 6, 11 and 12 were rejected under 35 U.S.C. § 102(e) as being anticipated by **Paul et al. [Paul]** (U.S. Patent No. 7,036,037). With respect to claim 1, Applicant respectfully traverses this rejection for at least the following reasons.

The PTO provides in MPEP § 2131 that

> *"[t]o anticipate a claim, the reference must teach every element of the claim...."*

Therefore, with respect to claim 1, to sustain this rejection the **Paul** reference must contain all of the above claimed elements of the respective claims. However, contrary to the examiner's position that all elements are disclosed in the **Paul** reference, the latter reference does not disclose " ... estimation means ... wherein the estimated processing delay corresponds to a delay that is caused as a function of a processing activity induced in said data processing circuit by said input data pattern and control means ... controlling ... processing of the input data pattern ... according to the processing activity of said data processing circuit in response to said estimated processing delay" as is claimed in claim 1.

In contrast, while the method of **Paul** teaches "multi-bit de-skewing of parallel bus signals which includes receiving data comprising a multi-bit word and a training pattern," wherein "[t]he difference in propagation delays causes the arrival times of individual data bits at the destination receiver to be different," and wherein "[t]he difference between the bit arrival times at the receiver is referred to as skew," (See Paul Abstract; col. 1, lines 20-24), **Paul** does not teach or suggest an "... estimation means ... wherein the estimated processing delay corresponds to a delay that is caused as a function of a processing activity induced in said data processing circuit by said input data pattern and control means ... controlling ... processing of the input data pattern ... according to the processing activity of said data processing circuit in response to said estimated processing delay" as is claimed in claim 1 of the present application. Rather, **Paul** simply teaches monitoring the parallel bit data bus for the first word of the training control pattern, determining skew of the data bits on a word by word basis, and performing de-skewing of the bit lines of the parallel bit data bus, i.e., to de-skew data bits that may be skewed in their transmission along the parallel bit line data bus 105.

(See **Paul** at Col. 5, lines 45-66; and Col. 6, lines 8-18).

Therefore, the rejection is not supported by the **Paul** reference and should be withdrawn. Accordingly, claim 1 is allowable and an early formal notice thereof is requested. Dependent claims 6 and 11 depend from and further limit allowable independent claim 1 and therefore are allowable as well.

By this amendment, claim 12 has been amended in a similar manner with respect to the amendments to claim 1. Claim 12 is believed allowable over the **Paul** reference for reasons similar as stated herein above with respect to overcoming the rejection of claim 1. Accordingly, claim 12 is believed allowable and the rejection thereof should be withdrawn.

Rejection under 35 U.S.C. § 103

Claims 2-5, 7-10 and 13-14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over **Paul et al. [Paul]** (U.S. Patent No. 7,036,037).

With respect to claims 2-5 and 7-10, Applicant respectfully traverses this rejection for at least the following reason. Dependent claims 2-5 and 7-10 depend from and further limit allowable independent claim 1 and therefore are allowable as well.

With respect to claims 13-14, Applicant respectfully traverses this rejection for at least the following reason. Dependent claims 13-14 depend from and further limit allowable independent claim 12 and therefore are allowable as well.

Conclusion

Except as indicated herein, the claims were not amended in order to address issues of patentability and Applicants respectfully reserve all rights they may have

under the Doctrine of Equivalents. Applicants furthermore reserve their right to reintroduce subject matter deleted herein at a later time during the prosecution of this application or a continuation application.

It is clear from all of the foregoing that independent claims 1 and 12 are in condition for allowance. Dependent claims 2-11 depend from and further limit independent claim 1, and therefore are allowable as well. Dependent claims 13-14 depend from and further limit independent claim 12, and therefore are allowable as well. The amendments herein are fully supported by the original specification and drawings as discussed herein; therefore, no new matter is introduced.

An early formal notice of allowance of claims 1-14 is requested.

Respectfully submitted,

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